AMENDMENTS TO THE CLAIMS

1-73. (Canceled)

74. (Currently amended) A two-stage memory device control circuit comprising:

a first signal node disposed on a first side of an array of memory devices;

a second signal node disposed on a second side of said array of memory devices;

a first logic gate circuit having a first output coupled to said first signal node;

a second logic gate circuit having a second output coupled to said second signal node;

a third logic gate circuit having a third output coupled to a first input of said first logic gate circuit;

a fourth logic gate circuit having a fourth output coupled to a second input of said second logic gate circuit;

a ~~third~~ section selection signal node mutually coupled to a third input of said third logic gate circuit and to a fourth input of said fourth logic gate circuit; and

a ~~fourth~~ global signal node mutually coupled to a fifth input of said third logic gate circuit and to a sixth input of said fourth logic gate circuit, wherein said ~~fourth~~ global signal node is signalingly equidistant from said fifth and sixth inputs.

75. (Previously presented) A global signal line memory triggering system comprising:

a first triggering circuit, said first triggering circuit being adapted to trigger a first sense amplifier at a first location of a memory array, said first triggering circuit including first and second NAND gates;

a second triggering circuit, said second triggering circuit being adapted to trigger a second sense amplifier at a second location of said memory array, said second triggering circuit including third and fourth NAND gates;

a selection node electrically coupled to said first and second triggering circuits at respective first and second inputs and adapted to receive a selection signal during a first time interval; and

a global signal node electrically coupled to said first and second triggering circuits at respective third and fourth inputs, said global signal node being disposed electrically equidistant from said third and fourth inputs, said global signal node being adapted to receive a global signal during a second time interval within said first time interval.

76. (Previously presented) A global signal line memory triggering system as defined in claim 75, wherein said third and fourth inputs comprise respective inputs of said second and fourth NAND gates.

77. (Currently amended) A signaling circuit comprising:

a first signal line disposed proximate to a first side of an array of memory cells;

a second signal line disposed proximate to a second side of said array of memory cells;

a first logic gate having a first output and first input, said first output being coupled to said first signal line;

a second logic gate having a second output and a second input, said second output being coupled to said second signal line;

a third logic gate having a third output coupled to said first input, said third logic gate having a third input and a fourth input, said third input being coupled to a section selection signal node;

a fourth logic gate having a fourth output coupled to said second input, said fourth logic gate having a fifth input and a sixth input, said fifth input being coupled to said section selection signal node;

a global signal node mutually coupled to said fourth and sixth inputs at a point electrically equidistant therebetween such that, respective first and second output signals are received substantially simultaneously at said first and second signal lines respectively when a global signal is received at said global signal node during a time interval when a selection signal is received at said selection signal node.

78. (Previously presented) A signaling circuit as defined in claim 77 wherein said first and second sides are disposed in substantially parallel spaced relation to one another.

79. (Previously presented) A signaling circuit as defined in claim 77 wherein send first, second, third and fourth logic gates are all NAND gates.

80. (Previously presented) A signaling circuit as defined in claim 77 wherein said first and second signal lines are coupled to respective first and second sense amplifiers.

81. (Previously presented) A signaling circuit as defined in claim 77 wherein said global signal comprises an equalization signal.

82. (Previously presented) A signaling circuit as defined in claim 77 wherein said global signal comprises an N sense amplifier trigger signal (NSA).

83. (Previously presented) A signaling circuit as defined in claim 77 wherein said global signal comprises A P said that the fire trigger signal (PSA).

84. (Previously presented) A sense amplifier comprising:

an NSA node, a PSA node, and an equalization node, said NSA node being coupled to a first tree structured signal routing circuit, said PSA node being coupled to a second tree structured signal routing circuit, and said equalization node being coupled to a third tree structured signal routing circuit.